Notice of Allowability	Application No.	Applicant(s)	
	10/770,899	JUENGLING ET AL.	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspond nce address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/3/2004*.

2. ☒ The allowed claim(s) is/are *1-7*.

3. ☒ The drawings filed on *03 February 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3/7/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This response is in reply to applicant's filing of 2/3/2004.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John D. Reed on June 10, 2004.

Please replace Claims 1 and 7 with revised Claims 1 and 7 as shown below.

1. A method of fabricating a semiconductor wafer, comprising:

providing a generally planar semiconductor wafer substrate such that said substrate is defined by substantially orthogonal first and second in-plane dimensions;

defining a topographic layer of conductive lead line material such that said topographic layer projects onto said substrate to occupy at least a portion of said substantially orthogonal first and second in-plane dimensions;

depositing at least one said topographic layer of conductive lead line material on said substrate;

depositing a plurality of topographic fill patterns adjacent either said topographic layer of conductive lead line material or another of said plurality of topographic fill patterns such that spaces defined therebetween possess substantially equal width as any other space;

arranging said plurality of topographic fill patterns and said at least one said topographic layer of conductive lead line material so that a grid defined by a plurality of crossings of said spaces contains no linear dimension longer than the longest

dimension of any one of said plurality of topographic fill patterns, and that no intersection defined by any of said plurality of crossings includes uninterrupted linear dimensions;

defining an array comprising said plurality of topographic fill patterns and topographic layers such that a substantially continuous straight-edged periphery around said array is defined by said topographic fill patterns and layers, and no portion of any of said topographic fill patterns overhangs a boundary of said array; and

depositing a planarization layer over said substrate such that it is disposed at least within said grid and laterally surrounds said at least one topographic layer of conductive lead line material and said plurality of topographic fill patterns.

7. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate;

depositing at least one topographic layer of conductive lead line material on said substrate;

depositing a plurality of topographic fill patterns adjacent either said topographic layer of conductive lead line material or another of said plurality of topographic fill patterns such that spaces defined therebetween possess substantially equal width as any other space;

arranging said plurality of topographic fill patterns and said at least one said topographic layer of conductive lead line material so that an array defining a plurality of valleys forms over said substrate and circumscribes at least one of said topographic fill patterns and said conductive lead line material, said array configured such that a substantially continuous straight-edged periphery *therearound is defined by* said plurality of topographic fill patterns, said conductive lead line material, or a combination of both, said array further configured such that no portion of any of said topographic fill patterns extends laterally beyond said periphery, and such that said topographic fill patterns and said conductive lead line material comprise a grid defined by a plurality of crossings of said spaces, said grid disposed within said array and containing no linear dimension longer than the longest dimension of any one of said plurality of topographic

fill patterns, and that no intersection defined by any of said plurality of crossings includes uninterrupted linear dimensions; and depositing a planarization layer over said substrate such that it is disposed at least within said grid.

Reasons For Allowance

3. Claims 1 – 7 are allowed.

4. The following is an examiner's statement of reasons for allowance.

Harvey (US 5,854,125) discloses (Figures 2d, 3a – 3c) a method of fabricating a semiconductor wafer, comprising: providing a generally planar semiconductor wafer substrate such that the substrate is defined by substantially orthogonal first and second in-plane dimensions, defining a topographic layer of conductive lead line material such that said topographic layer projects onto the substrate to occupy at least a portion of the substantially orthogonal first and second in-plane dimensions; depositing at least one topographic layer of conductive lead line material on the substrate, depositing a plurality of topographic fill patterns adjacent either the topographic layer of conductive lead line material or another of the plurality of topographic fill patterns such that spaces defined there between possess substantially equal width as any other space and depositing a planarization layer over the substrate such that it is disposed at least within the grid and laterally surrounds the at least one topographic layer of conductive lead line material and the plurality of topographic fill patterns.

The prior art does not teach or fairly suggest, in combination with the other claimed limitations, arranging said plurality of topographic fill patterns and said at least one said topographic layer of conductive lead line material so that a grid defined by a plurality of

crossings of said spaces contains no linear dimension longer than the longest dimension of any one of said plurality of topographic fill patterns; that no intersection defined by any of said plurality of crossings includes uninterrupted linear dimensions; and defining an array comprising said plurality of topographic fill patterns and topographic layers such that a substantially continuous straight-edged periphery around said array is defined by said topographic fill patterns and layers, and no portion of any of said topographic fill patterns overhangs a boundary of said array;

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled " Comments on Statement of Reasons for Allowance".

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takizawa (US 6,504,254) teaches a semiconductor device with dummy wiring layers.

Chen et al. (US 6,178,853 B1) teaches a method of designing active patterns with a shifted dummy pattern.

Gabriel et al. (US 5,861,342) teaches a method of improving the planarity of spin on glass layers.

Findley et al. (US 5,763,955) teaches integrated filled layers for integrated circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2813

June 11, 2004

Tuan H. Nguyen

Tuan H. Nguyen
Primary Examiner